IN THE CLAIMS

Kindly replace the claims of record with the following full set of claims:

1. (Currently amended) A data processing system[[,]] comprising:

memory device and a plurality of data processors provided for accessing to said memory device, wherein a communication interface is coupled between said memory device and said plurality of data processors, said communication interface including:

a network of nodes and a memory interface, each node comprising at least one slave port for receiving a memory access request from a data processor or from a previous node and at least one master port for issuing a memory access request to a next node or to said memory device in accordance with the memory access request received at said slave port, wherein one or more slave ports are connected to a master port of a previous node, wherein one or more slave ports are connected to one of said data processors, wherein one or more master ports are connected to a slave port of a next node, wherein one or more master ports are connected to the memory interface, wherein the memory interface arbitrates access to the memory device, wherein the communication interface is positioned on a single chip, and wherein the memory device is not positioned on the single chip, wherein said communication interface further includes at least one local memory unit adapted to be selectively accessed to by a memory access request, wherein said memory device and said local memory unit have a single address space and an address range within said single address space distinguishes between said memory device and said local memory.

2. (Previously presented) The data processing system according to claim 1, wherein at each node the number of said slave ports is higher than the number of said master ports.

3. (Previously presented) The data processing system according to claim 1, wherein said network of nodes is hierarchically structured.

4. (Previously presented) The data processing system according to claim 3, wherein

said network of nodes is arranged in a directed acyclic graph structure.

5. (Previously presented) The data processing system according to claim 4, wherein said network of nodes is arranged in a tree structure.

6. (Previously presented) The data processing system according to claim 1, wherein said network of nodes include n groups of nodes with $n \geq 2$, wherein each of the slave ports of the nodes of a first group is connected to one of said plurality of data processors, the master ports of the nodes of the n^{th} group are coupled to said memory device, and each of the slave ports of the nodes of the n^{th} group is connected to a master port of the nodes of the $(n-1)^{th}$ group.

7. (Previously presented) The data processing system according to claim 1, wherein said nodes are hubs.

8. (Cancelled).

9. (Currently amended) The data processing system according to claim [[8]] 1, wherein at least one node further comprises at least one memory port to which a local memory unit is connected.

10. (Currently amended) The data processing system according to claim [[8]] 1, wherein said communication interface includes a cache controller for controlling at least a section of the local memory unit as a cache memory.

11. (Previously presented) The data processing system according to claim 1, wherein said communication interface further includes at least one synchronization means for streaming communication between data processors.

12. (Previously presented) The data processing system according to claim 11, wherein at least one node includes said synchronization means for streaming

communication between the data processors directly or indirectly coupled to said nodes.

13. (Previously presented) The data processing system according to claim 11, wherein the local memory unit is configured to provide storage based on a first-in/first-out function and said synchronization means comprises a first-in/first-out administration means for controlling said local memory unit.

14. (Cancelled).

15. (Currently amended) The data processing system according to claim [[14]] 1, wherein at least a portion of said plurality of data processors is positioned on said single chip.